REMARKS

Claims 1-19 are pending. Claims 1-4 and 12-16 have been amended. No new matter has been added. The specification supports that *aligning the frame includes controlling a timing signal indicating a bus cycle that contains the beginning of the frame and shifting the received data sequence so that the beginning of the frame occurs at bit zero of the bus cycle* at least on page 5. Reconsideration and allowance of all pending claims are requested.

Specification Objection:

The title is objected to for allegedly being not descriptive. The title has been amended to "A Frame Aligning Deframer" to obviate the contention. However, should the Examiner have any suggestions or a more descriptive title, these suggestions would be appreciated.

35 U.S.C. § 102 Rejections:

Claims 1, 3, 5, 9-12, 14, and 17-18 stand rejected under 35 U.S.C. § 102(e) for allegedly being anticipated by US Patent No. 6,359,933 to Aslanis et al. ("Aslanis").

Aslanis does not teach or suggest each and every element of claim 1. For example, Aslanis fails to teach or suggest ***determining whether a total number of comparison errors exceeds***

a tolerance threshold that is greater than zero, as recited in claim 1. When the received data sequence is compared against a portion of a predetermined sequence, each mismatch is measured as an error in claim 1. In contrast, Aslanis teaches making a distinction between situations where excessive noise "produces a poor correlation result, even though there is no actual loss of frame synchronization" and situations where an actual loss of frame synchronization has occurred. *See* col. 8, ll. 5-20. In making the distinction, Aslanis performs a "correlation" between "contents of synchronizing frame" and "synchronizing sequences supplied from the store 58 via the weighting multiplier 60." Col. 8, ll. 25-44.

In general, a correlation is a statistical measure between two random variables that indicates the strength and direction of a linear relationship between the two random variables. Larger correlation results indicated greater linear relationship between the variables. Aslanis acknowledges this by disclosing that "a large correlation result indicates frame synchronization has been maintained, and a smaller correlation result indicates a loss of frame synchronization." Col. 3, ll. 23-26. However, the correlation result in Aslanis does not determine the ***total number of comparison errors*** as recited in claim 1. The

correlation in Aslanis "consists of a multiplication of each complex amplitude supplied from the output of the FEQ in the unit 40 by a corresponding complex amplitude of the synchronizing sequence from the store 58, weighted by the multiplier 64 in accordance with a respective weighing factor as described below, and a summation of the real parts of the complex amplitude products to produce a single real correlation result at the output of the correlator 60." Col. 8, ll. 36-44. Therefore, the multiplication required in determining the correlation result in Aslanis is not making comparisons, and Aslanis cannot reasonably be construed to disclose ***determining whether a total number of comparison errors exceeds a tolerance threshold that is greater than zero*** as recited in claim 1.

In addition, Aslanis does not disclose ***aligning the frame if the threshold is not exceeded*** as recited in claim 1. In Aslanis, a correlation result that ***exceeds the threshold*** indicates that the synchronization has been maintained. *See Fig. 2.* Thus, Aslanis discloses that no action is taken when the correlation result exceeds the threshold. Col. 9, ll. 7-23. In contrast, claim 1 recites ***aligning the frame if the threshold is not exceeded***. In other words, when the threshold is ***not exceeded***, the received data sequence and the portion of a

predetermined sequence match, and thus an alignment of the frame can be performed. Since the correlation result in Aslanis is unrelated to the total number of comparison errors, the threshold in Aslanis represents a different measurement than the threshold as recited in claim 1.

Further, Aslanis fails to disclose ***wherein aligning includes controlling a timing signal indicating a bus cycle that contains the beginning of the frame and shifting the received data sequence so that the beginning of the frame occurs at bit zero of the bus cycle*** as recited in claim 1. Aslanis is silent to the recited features.

For at least these reasons, claim 1 is patentable over Aslanis.

Claims 12 and 14 recite similar elements to those recited in claim 1, and thus are patentable over Aslanis for at least the reasons set forth with respect to claim 1. In addition, claims 3, 5, 9-11 and 14 depend from claims 1 and 12, and thus are patentable over Aslanis for at least the reasons set forth with respect to claims 1 and 12 above. The dependent claims 3, 5, 9-11 and 14 are additionally patentable over Aslanis for independent reasons.

For example, in regard to claim 3, Aslanis fails to disclose that ***the portion of the received data sequence and the portion of the predetermined sequence are compared in multi-bit symbols, and the total number of comparison errors comprises the number of symbols that are not perfectly matched*** as recited in claim 3. Although the Office Action alleges that Aslanis discloses the features at col. 4, ll. 34-35, the cited portion and any other portions of Aslanis fail to disclose the features. Aslanis discloses using ***multicarrier symbols*** and not ***multi-bit symbols*** as recited in claim 3. Col. 4, ll. 34-35. In addition, as set forth with respect to claim 1 above, the correlation result in Aslanis is determined using ***multiplication***, which is unrelated to making comparisons or determining the total number of comparison errors. Further, since determining the total number of comparison errors are not disclosed or suggested in Aslanis, the correlation result in Aslanis cannot reasonably be construed to teach or suggest that ***the total number of comparison errors comprises the number of symbols that are not perfectly matched*** as recited in claim 3. In fact, Aslanis is silent as to determining if any perfectly matched symbols exists as recited in claim 3.. The correlation result in Aslanis is entirely unrelated to determining perfectly matched symbols.

For at least these additional reasons, claim 3 is patentable over Aslanis. Claim 14 recites similar features, and thus is also patentable for at least the reasons set forth with respect to claim3 above.

In regard to claim 5, Aslanis fails to disclose ***comparing a second portion of the received data sequence to a second portion of the predetermined sequence; determining a second total number of comparison errors based on the second comparison; and determining whether the second total number of comparison errors exceeds a second tolerance threshold*** as recited in claim 5. Aslanis teaches determining the ***correlation result*** for additional synchronous frames, and the correlation result is unrelated to comparing received data sequence with the predetermined sequence. In addition, just as the total number of comparison errors are not determined for the first portion of the received data sequence, Aslanis does not disclose determining a total number of comparison errors based on the second comparison as recited in claim 5. Also, Aslanis does not teaches or suggests a second threshold as recited in claim 5. Further, the Office Action admits that Aslanis fails to teach or suggest "comparing a second portion of received data" *See Office*

Action, pg. 7, ¶ 26. For at least these additional reasons, claim 5 is patentable over Aslanis.

In regard to claim 17, Aslanis fails to teach or suggest ***parallel compare circuits configured to receive data and a predetermined sequence, and to produce a comparison result*** as recited in claim 17. The Office Action alleges that "[b]uffer, 36, acts as a serial-to-parallel converter." *See Office Action, pg. 4, ¶ 12.* The parallel-to-serial converter buffer 36 in Aslanis is a standard serial data interface to parallel data interface converter. This buffer is irrelevant to the claimed ***parallel compare circuits***. In contrast, the ***parallel compare circuits*** as recited in claim 17 are multiple compare circuits arranged in parallel in order to perform multiple comparisons in parallel. *See Applicant's FIGS. 2 and 3.* Therefore, the buffer in Aslanis is entirely unrelated to the claimed ***parallel compare circuits*** as recited in claim 17. In addition, the buffer 36 in Aslanis is a storage device used to "determine which sequences, each of 512 time domain samples, are supplied to the FFT unit 38 to be transformed into respective frequency domain multicarrier symbols." Col. 6, ll. 36-41. In other words, the buffer holds the data to be converted from time domain to frequency domain. This transformation in Aslanis from the time domain to the

frequency domain is not performing a comparison as recited in claim 17. Therefore, the buffer in Aslanis does not compare the data and the predetermined sequence and to produce a comparison result as recited in claim 17.

Aslanis also fails to teach or suggest ***a state machine configured to receive the comparison result from the parallel compare circuits and to produce a frame alignment determination*** as recited in claim 17. The Office Action alleges that the decision unit 68 in Aslanis is a state machine. *See Office Action, pg. 4, ¶ 12.* However, the decision unit 68 cannot reasonably construed as the state machine recited in claim 17. Aslanis discloses, in FIG. 1, that the decision unit 68 receives the correlation result from the correlator 60 and not the buffer 36. This contention conflicts with the Office Action's own assertion that buffer 36 is the parallel comparison circuits. Thus, the decision unit 68 cannot reasonably be construed as the ***state machine*** recited in claim 17.

In regard to claim 18, Aslanis fails to teach or suggest ***each of the parallel compare circuits is configured to produce a separate comparison result*** as recited in claim 18. Similar to the claim 17, the buffer 68 is entirely unrelated to the parallel compare circuits. For example, the buffer 68 is a

single buffer incapable of reasonably being construed as ***each of the parallel compare circuits***. Therefore, claim 18 is patentable over Aslanis for at least the reasons set forth with respect to claim 17 above.

Claims 1-2, 4 and 12-13 are rejected under 35 U.S.C. 102(b) as allegedly being anticipated by US Patent No. 6,081,570 to Ghuman et al. ("Ghuman").

Ghuman fails to disclose ***wherein aligning includes controlling a timing signal indicating a bus cycle that contains the beginning of the frame and shifting the received data sequence so that the beginning of the frame occurs at bit zero of the bus cycle*** as recited in claim 1. While Ghuman discloses that "data is aligned to the byte boundaries of a data frame (*See, Col. 15, ll. 57-58*), Ghuman is silent to the recited features of claim 1. For at least this reason, claim 1 is patentable over Ghuman.

Claim 12 recites similar features of claim 1 and thus is patentable over Ghuman for at least the reason set forth with respect to claim 1 above. In addition, claims 2, 4 and 13 depend from claims 1 and 12, and thus are patentable over Ghuman

for at least the reasons set forth with respect to claims 1 and 12 above.

35 U.S.C. § 103 Rejections:

Claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ghuman.

Claim 15 recites similar features as claim 1 and thus is patentable for at least the reason set forth with respect to claim 1 above. Claim 16 depends from claim 15 and thus is patentable over Ghuman for at least the reason set forth with respect to claim 15.

Claims 5-8 and 19 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Aslanis in view of Tsubaki.

Aslanis fails to teach or suggest each and every feature of independent claims 1 and 17 as set forth above. The Office Action does not assert that the addition of Tsubaki alleviates the deficiencies of Aslanis with respect to the recited features of the independent claims 1 and 17. Since claims 5-8 and 19 depend from claims 1 and 17 respectively, the proposed combination of Aslanis and Tsubaki fails to teach or suggest each and every feature of claims 5-8 and 19. Thus, claims 5-8

and 19 are patentable over the proposed combination of Aslanis and Tsubaki for at least the reasons set forth with respect to claims 1 and 17 above. In addition, claims 5-8 and 19 are independently patentable.

For example, in regard to claim 19, the Office Action admits that Aslanis fails to disclose "an additional compare circuit not in parallel with the parallel compare circuit, the additional compare circuit being configured to receive data and the predetermined sequence and to produce another comparison result which the state machine is further configured to receive . *See Office Action, pg. 8, ¶ 30.* Although the Office Action alleges that Tsubaki teaches the features in FIG. 3, the addition of Tsubaki does not alleviate the deficiencies of Aslanis. Tsubaki teaches a single frame sync detector 3 in FIG. 3 and does not teach the parallel compare circuits as recited in claim 19. Tsubaki does not disclose or suggest a non-parallel connection for the frame sync detector since there are no parallel compare circuits connected with the frame sync detector. For at least this additional reason, claim 19 is patentable over the proposed combination of Aslanis and Tsubaki.

Conclusion

It is believed that all of the pending claims have been addressed in this paper. However, failure to address specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Claims 1-19 are in condition for allowance, and a notice to that effect is respectfully solicited. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-5070.

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No fees are believed to be due. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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